ABSTRACT OF THE INVENTION

A flash memory structure. The structure includes device isolation regions defined on an active area of a substrate, a deep well of first conductive type, stacked gate structures, a tunneling oxide layer, wells of second conductive type, sources and drains, wherein the aforementioned deep well of first conductive type is located in the active area and below the device isolation regions. The aforementioned wells of second conductive type are formed in the area corresponding to the drains and below the device isolation regions between the adjacent stacked gate structures. The aforementioned sources and drains are in the active areas located on both sides of the control gates, wherein the drains are enclosed by the wells of second conductive type; and the sources are located on both sides of the wells of second conductive type and electrically connected with each other via the deep well of first conductive type. Moreover, the present invention also provides a fabrication method and an operating method for the aforementioned structure.